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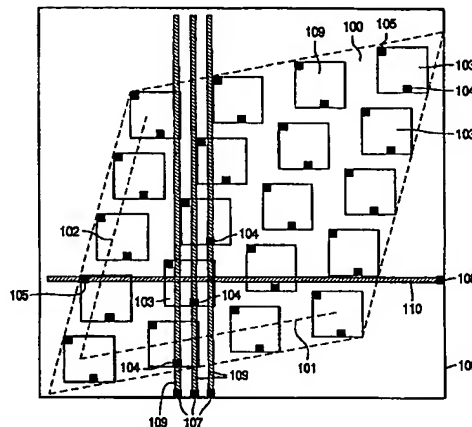
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[Continued on next page]

(54) Title: DEVICE FOR PARALLEL DATA PROCESSING AS WELL AS A CAMERA SYSTEM COMPRISING SUCH A DEVICE



(57) Abstract: The invention relates to a device for parallel data processing, a DSP. The device according to the invention comprises a processor matrix (100) in which processors (103) are arranged in rows (101) and columns (102). Furthermore, the device (100) comprises first and second external data ports (107, 108). The rows (101) arranged in a stepwise manner and the columns are arranged in a stepwise manner. The processors (103) have a first processor data port (104), which is connected with one of the first external data ports (107) by means of first essentially straight connection. The processors (103) further comprise a second processor data port (105), which is connected with one of the second external data ports (108) by means of an essentially straight second connection (110). The first connection (107) and the second connection (108) are oriented substantially orthogonal to each other. A problem associated with conventional DSPs is that the connections to and from the processors within the DSP take up large amounts of silicon area. By arranging both rows and columns of the DSP according to the invention in a stepwise manner the connections may be essentially straight, thus minimizing their lengths and thus the surface area occupied.

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## INTERNATIONAL SEARCH REPORT

03/50018

## A. CLASSIFICATION OF SUBJECT MATTER

IPC 7 G06F15/80 H04N9/04

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

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Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the International search (name of data base and, where practical, search terms used)

EPO-Internal

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Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	SEQUIN C H: "DOUBLY TWISTED TORUS NETWORKS FOR VLSI PROCESSOR ARRAYS" PROCEEDINGS OF THE ANNUAL SYMPOSIUM ON COMPUTER ARCHITECTURE. MINNEAPOLIS, MAY 12 - 14, 1981, PROCEEDINGS OF THE ANNUAL INTERNATIONAL SYMPOSIUM ON COMPUTER ARCHITECTURE, LONG BEACH, IEEE, US, vol. SYMP. 8, 1 May 1981 (1981-05-01), pages 471-480, XP000745285 figure 10	1
A	US 5 752 068 A (GILBERT ET AL) 12 May 1998 (1998-05-12) column 4, line 35 - line 45 column 5, line 34 - line 51; figure 2 column 15, line 7 - line 15 ----- -/--	1-11

☒ Further documents are listed in the continuation of box C.☒ Patent family members are listed in annex.

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Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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